UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,756	11/03/2003	Albert Sun	MXIC 1521-1	4258

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ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

	Application No.	Applicant(s)
Office Action Summary	10/699,756	SUN ET AL.
	Examiner	**Art Unit**	
	Hetul Patel	2186	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>03</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on <u>26 January 2007</u>.

2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) <u>1-17</u> is/are pending in the application.

   4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) <u>1-17</u> is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   a)☐ All b)☐ Some * c)☐ None of:

     1.☐ Certified copies of the priority documents have been received.

     2.☐ Certified copies of the priority documents have been received in Application No. _____.

     3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
   Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1.   This office action is in response to arguments filed on January 26, 2007. Claims

1-17 are presented again for examination.

2.   The petition filed on January 26, 2007 to revive application has been granted and

the prosecution is re-opened.

3.   It is unclear why the USPN: 4972105 has been submitted with the response.

4.   Applicant's arguments filed on January 26, 2007 have been fully considered and

they are persuasive. Therefore, the rejection has been withdrawn. However, upon

further consideration, a new ground(s) of rejection is made in view of Ikeda et al.

(USPN: 2003/0184339).

Terminal Disclaimer

5.   The terminal disclaimers filed on 04/05/2006 disclaiming the terminal portion of

any patent granted on this application which would extend beyond the expiration date of

any patent(s) granted on application numbers 10/699,766 and 10/699,764 have been

reviewed and are accepted. The terminal disclaimers have been recorded.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by
another filed in the United States before the invention by the applicant for patent or (2) a patent
granted on an application for patent by another filed in the United States before the invention by the

applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6.   Claims 1-3, 5-7, 12-15 and 17 are rejected under 35 U.S.C. 102(e) as being

anticipated by Ikeda et al. (USPN: 2003/0184339) hereinafter, Ikeda.

As per claim 1, Ikeda teaches an integrated circuit (i.e. the system LSI 10 in Fig.

1) comprising: an input port (i.e. shown in Fig. 1 connecting device 2 and 15) by which

data is received from a source (i.e. the DRAM 2 in Fig. 1) external to the integrated

circuit (e.g. see Fig. 1); a configurable logic array (i.e. the Offchip FPGA 14 in Fig. 1)

having a programmable configuration defined by configuration data stored in electrically

programmable configuration points within the configurable logic array; memory (i.e. the

RAM or ROM for storing the execution program 3 shown in Fig. 1) storing instructions

for a mission function for the integrated circuit, storing instructions for a configuration

load function used to receive configuration data via said input port, and storing

instructions for an initialization function used to transfer the configuration data to the

programmable configuration points within the configurable logic array in response to an

initialization event; and a processor (i.e. the RISC processor 11 in Fig. 1) coupled to the

memory which fetches and executes said instructions from the memory (e.g. see

paragraphs [0051]-[0052] and Fig. 1).

As per claims 2, Ikeda teaches the claimed invention as described above and

furthermore, Ikeda teaches a programmable non-volatile configuration memory (i.e. the

ROM for storing the execution program 3 shown in Fig. 1) adapted to store the

configuration data. Wherein the initialization function transfers the configuration data

from the programmable configuration memory to the configurable logic array (e.g. see Fig. 1).

As per claims 3 and 5, Ikeda teaches the claimed invention as described above and furthermore, Ikeda teaches that the memory (i.e. the ROM for storing the execution program 3 shown in Fig. 1) comprises a nonvolatile read-only memory (i.e. the ROM) (e.g. see Fig. 1).

As per claims 6 and 7, Ikeda teaches the claimed invention as described above. In order to load/receive data from external device(s) and transferring the data within the FPGA, the initialization function/instruction, the load function/instruction and the transfer function/instruction has to be stored in the memory so the processor can execute/run it.

As per claims 12-13, Ikeda teaches the claimed invention as described above and furthermore, Ikeda teaches that the electrically programmable configuration points comprise nonvolatile, charge programmable memory cells and nonvolatile, programmable memory cells (i.e. the offchip FPGA 14 in Fig. 1).

As per claims 14, Ikeda teaches the claimed invention as described above and furthermore, Ikeda teaches that the integrated circuit further comprises an interface (i.e. the combination of 17, 18, 20 and 21 in Fig. 1) between the processor (i.e. 11 in Fig. 1) and the configurable logic array (i.e. 14 in Fig. 1) supporting the configuration load function (e.g. see Fig. 1).

As per claims 15, Ikeda teaches the claimed invention as described above and furthermore, Ikeda teaches that the memory (i.e. the RAM or ROM for storing the

execution program 3 shown in Fig. 1) stores instruction for an in-circuit programming

function to write/modify instructions for the initialization function (e.g. see Fig. 1).

As per claims 17, Ikeda teaches the claimed invention as described above and

furthermore, Ikeda teaches that the processor comprises a configurable logic array (i.e.

the offchip FPGA 14 in Fig. 1) configured to execute the instructions (e.g. see Fig. 1).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7.   Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda in

view of Hsu et al. (USPN: 5,359,570) hereinafter, Hsu.

As per claim 4, Ikeda teaches that the memory comprises a nonvolatile read-only

memory (i.e. the ROM for storing the execution program 3 shown in Fig. 1). However,

Ikeda does not teach that the memory comprises a floating gate memory device. Hsu,

on the other hand, teaches that floating gate memory devices have the advantage over

using the ROM that they can be programmed and erased, electrically, thereby,

exhibiting the advantages of ROM memory, i.e., low power consumption and faster

access, along with the writeability of magnetic medium. In addition, as integrated circuit

fabrication scale increases, greater density can be achieved. Therefore, it would have

been obvious to combine Hsu and Ikeda for the benefits described above.

8.   Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Ikeda in view of Sun et al. (USPN: 6,401,221) hereinafter, Sun.

As per claims 8 and 9, Ikeda teaches that the claimed invention as described

above, but failed to teach the watchdog timer as claimed. Sun, however, discloses a

watchdog timer coupled to the CPU (i.e. 122 in Fig. 1), an initialization function that

includes using a timer to generate an initialization event on a response to an error, upon

the initialization event, reexecuting the initialization function (column 4, lines 15-19).

Ikeda and Sun et al. are analogous art because they are from the same field of

endeavor, an in circuit programming system that can run downloaded code and reset

the system when necessary. At the time of the invention it would have been obvious to

a person of ordinary skill in the art to incorporate a watchdog timer and the functions

that come with the timer. The suggestion for doing so would have been the ability to

reset the system when an error occurs. Therefore, it would have been obvious to

combine Sun and Ikeda for the benefit of resetting the system by reloading the

configuration data to obtain the invention as specified in claims 8 and 9.

9.   Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda in

view of Sun et al. (USPN: 5,901,330) hereinafter, Sun2.

As per claim 10, Ikeda teaches that the claimed invention as described above,

but failed to teach that the initialization function includes receiving encrypted

configuration data via an input port on the integrated circuit, and decrypting the

configuration data. Sun2, however, discloses that the initialization/configuration load

function includes receiving encrypted configuration data via the input port and then

decrypting the configuration data (column 13, lines 59-66). Ikeda and Sun2 are

analogous art because they are from the same field of endeavor, an in circuit

programming system that can run downloaded code and reset the system when

necessary. At the time of the invention it would have been obvious to a person of

ordinary skill in the art to encrypt the incoming data and then decrypt the data. The

suggestion for doing so would have been system security. Therefore, it would have

been obvious to combine Sun2 and Ikeda for the benefit of security to obtain the

invention as specified in claims 10. The examiner notes that the in-circuit programming

and the initialization function perform the same function and are therefore not dissimilar

enough to differentiate given the known definitions of the two terms.

10.   Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda in

view of Lawman (USPN: 6,028,445).

        As per claim 11, Ikeda teaches that the claimed invention as described above,

but failed to teach that the initialization function includes receiving compressed

configuration data via an input port on the integrated circuit, and uncompressing the

configuration data. Lawman, however, discloses a initialization function that includes

receiving compressed configuration data via an input port and then decompressing the

data (column 8, lines 12-33). Ikeda and Lawman are analogous ad because both deal

with downloading data in a compressed format to a programmable device. At the time of

the invention it would have been obvious to a person of ordinary skill in the art to allow

the initialization function to receive compressed data and to decompress it. The suggestion for doing so would have been to save time and bandwidth. Therefore, it would have been obvious to combine Lawman and Ikeda for the benefit of time and bandwidth savings to obtain the invention as specified in claims 11.

11.   Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda in view of Akao et al. (USPN: 5,900,008) hereinafter, Akao.

As per claim 16, Ikeda teaches that the claimed invention as described above, but failed to teach that the memory include a protected memory array storing instructions for a first configuration load function, a second memory array storing instructions for a second configuration load function, the first memory array protected from alteration by a programming function, and the second memory accessible to be written/modified by the programming function.

Akao, on the other hand, teaches the memory include a protected memory array storing instructions for a first configuration load function, a second memory array storing instructions for a second configuration load function, the first memory array protected from alteration by a programming function, and the second memory accessible to be written/modified by the programming function (e.g. see the Abstract). Ikeda and Akao are analogous art because they are from a similar problem solving area, processing systems that employ program areas and protection for some of the areas. At the time of the invention it would have been obvious to a person of ordinary skill in the ad to add a protected memory area. The suggestion for doing so would have been protect the data

from accidental or malicious overwrites/deletes. Therefore, it would have been obvious

to combine Akao and Ikeda for the benefit of data protection to obtain the invention as

specified in claim 16. The examiner notes that Akao does not expressly state protecting

the first configuration load function or not protecting the second configuration load

function, but that combining Akao and Ikeda would give anyone with skill in the art

motivation to protect one of the configuration load functions.

Conclusion

12.   The prior art made of record and not relied upon is considered pertinent to
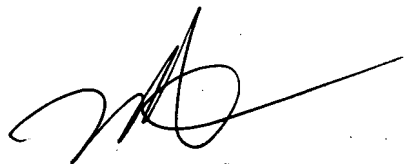
applicant's disclosure.

> ➢ Synder (USPN: 7,185,162) discloses the claimed invention, i.e. a flash
>
>   memory within an IC which loads data from an external memory to an internal
>
>   memory and a processor within the IC executes the instruction from the
>
>   internal memory.

13.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Hetul Patel whose telephone number is 571-272-4184.

The examiner can normally be reached on 8:00 - 5:30.

        If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

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USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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